VERIFICATION OF TRANSLATION

I, the below named translator, hereby declare:

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that I am knowledgeable in the English and Japanese languages and that I believe the following is a true and complete translation into the English language of Japanese Patent Application No. 2000 - 394040 filed at the Japanese Patent Office on the 26th day of December, 2000 for Letters Patent, including a true translation of the Official Certificate of the Application.

Signed this 1st day of December, 2003

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[Translation of Priority Certificate]

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[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

[Claim]

[Claim 1]

A semiconductor device in which a bonding pad electrode is formed by stacking a cover insulating film on a lower metal layer, by forming an opening in said cover insulating film to expose said lower metal layer and by covering the exposed lower metal layer with an upper electrode layer made of material having corrosion resistance against substance which is corrosive to said lower electrode layer,

characterized in that a step portion is provided in said cover insulating film by making the size of an upside portion of said opening of said cover insulating film larger than the size of a down side portion of said opening, and said upper electrode layer overlaps a step surface of said step portion.

[Claim 2]

A semiconductor device as set forth in claim 1, wherein said cover insulating film comprises a lower layer silicon nitride film and an upper layer PSG film, and said step surface is a surface of said silicon nitride film.

[Claim 3]

A semiconductor device as set forth in claim 1, wherein said cover insulating film comprises a PSG film.

[Claim 4]

A semiconductor device as set forth in any one of claims 1-3, wherein said lower electrode layer comprises a metal film of aluminum system, and said upper electrode layer comprises a metal film which has corrosion resistance against substance corrosive to aluminum.

[Claim 5]

A semiconductor device as set forth in claim 4, wherein said upper electrode layer comprises a TiNiAg film.

[Claim 6]

A semiconductor device as set forth in claim 4 or 5, wherein a high conductivity metal plate is coupled onto said bonding pad electrode via a conductive paste.

[Claim 7]

A semiconductor device as set forth in claim 6, wherein said conductive paste is an Ag paste, and said high conductivity metal plate is a copper plate.

[Claim 8]

A semiconductor device as set forth in claim 6 or 7, wherein said bonding pad electrode is a source pad electrode of a power MOSFET.

[Claim 9]

A method of manufacturing a semiconductor device in which a bonding pad electrode is formed by stacking a cover insulating film on a lower metal layer, by forming an opening in said cover insulating film to expose said lower metal layer and by covering the exposed lower metal layer with an upper electrode layer made of material having corrosion resistance against substance which is corrosive to said lower electrode layer,

characterized in that said method comprises: providing a step portion in said cover insulating film by making the size of an upside portion of said opening of said cover insulating film larger than the size of a down side portion of said opening, and forming said upper electrode layer such that said upper electrode layer overlaps a step surface of said step portion.

[Claim 10]

A method of manufacturing a semiconductor device as set forth in claim 9, wherein forming said step portion is performed by side-etching said cover insulating film by isotropically etching said cover insulating film by using a photo resist pattern as a mask, and wherein forming said upper electrode layer is performed by using a lift-off method in which said photo resist pattern is used as a mask.

[Claim 11]

A method of manufacturing a semiconductor device as set forth in claim 10, wherein, as said cover insulating film, a lower layer silicon nitride film and an upper layer PSG film are stacked, said side-etching is performed on said PSG film, thereafter said silicon nitride film is plasma etched by using said photo resist pattern as a mask, thereby exposing via said PSG film a surface of said silicon nitride film as said step surface, wherein said upper layer electrode layer is formed thereon, thereafter the upper layer electrode layer on said photo resist pattern is removed by using said lift-off method, thereby said upper layer electrode layer is left

unremoved on the portion of said lower electrode layer exposed by said opening of said PSG film and of said silicon nitride and on said step surface.

[Claim 12]

A method of manufacturing a semiconductor device as set forth in claim 10, wherein, as said cover insulating film, a lower layer silicon nitride film is stacked, said silicon nitride film is plasma etched by using a first photo resist pattern as a mask, thereby an opening of said silicon nitride film is formed which exposes said lower layer electrode layer, wherein, after removing said first photo resist pattern, a PSG film is formed thereon, said side-etching is performed on said PSG film by using a second photo resist pattern having an opening wider than the opening of said silicon nitride film as said photo resist pattern, thereby a surface of said silicon nitride film exposed via said PSG film becoming said step surface, wherein said upper layer electrode layer is formed thereon, thereafter the upper layer electrode layer on said second photo resist pattern is removed by using said lift-off method, thereby said upper layer electrode layer is left unremoved on the portion of said lower electrode layer exposed by said opening of said PSG film and of said silicon nitride and on said step surface.

[Claim 13]

A method of manufacturing a semiconductor device as set forth in claim 10, wherein, as said cover insulating film, a PSG film is stacked, said PSG film is anisotropically or isotropically etched by using a first photo resist pattern having an opening of a predetermined width as a mask, thereby a trench is formed in said PSG film, said PSG film is further isotropically etched by using a second photo resist pattern having an opening wider than the opening of said trench as a mask until said lower layer electrode layer is exposed from said trench, thereby forming said step surface at an end portion of the opening of said PSG film, wherein a film constituting said upper layer electrode layer is formed thereon, thereafter the upper layer electrode layer on said second photo resist pattern is removed by using said lift-off method, thereby said upper layer electrode layer is left unremoved on the portion of said lower electrode layer exposed by said opening of said PSG film and on said step surface.

[Claim 14]

A method of manufacturing a semiconductor device as set forth in any

one of claims 9-13, wherein said lower electrode layer comprises a metal film of aluminum system, and said upper electrode layer comprises a metal film which has corrosion resistance against substance corrosive to aluminum.

[Claim 15]

A method of manufacturing a semiconductor device as set forth in claim 14, wherein said upper electrode layer comprises a TiNiAg film.

[Claim 16]

A method of manufacturing a semiconductor device as set forth in claim 14 or 15, further comprising: coupling a high conductivity metal plate onto said bonding pad electrode via a conductive paste.

[Claim 17]

A method of manufacturing a semiconductor device as set forth in claim 16, wherein said conductive paste is an Ag paste, and said high conductivity metal plate is a copper plate.

[Claim 18]

A method of manufacturing a semiconductor device as set forth in claim 16 or 17, wherein said bonding pad electrode is a source pad electrode of a power MOSFET.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Pertains]

The present invention relates generally to a semiconductor device and a method of manufacturing the same. More particularly, the present invention relates to a semiconductor device having bonding pad electrode(s) of a multi-layer structure which have high corrosion resistance, and a method of manufacturing such semiconductor device.

[0002]

[Prior Art]

With respect to such kind of bonding pad electrode structure, an explanation will be made on a conventional example with reference to Fig. 9. In the drawing, a reference numeral 1 designates an aluminum film electrically coupled with a predetermined region of a semiconductor substrate (not shown in the drawing) on which a circuit element is formed. For example, if the circuit element is a MOSFET, the aluminum film 1 is a

source electrode electrically coupled with the source region. On the aluminum film 1, there is formed a cover insulating film 2 made, for example, of a PSG film, and an opening of the cover insulating film 2 is covered by, for example, a TiNiAg film 3 such that the TiNiAg film 3 overlaps the cover insulating film 2. Thereby, a bonding pad electrode structure is formed in which the aluminum film 1 is protected from a corrosive substance.

[0003]

The above-mentioned bonding pad electrode structure is fabricated as follows. That is, after forming the opening in the cover insulating film 2, the TiNiAg film 3 is deposited on whole area of the substrate. The TiNiAg film 3 comprises, for example, a Ti film having a thickness of 1000 angstroms, an Ni film having a thickness of 1000 angstroms and an Ag film having a thickness of 10000 angstroms. The TiNiAg film 3 is etched by masking an area wider than the area of the opening of the cover insulating film 2 by using a photo resist pattern of a photolithography method such that the TiNiAg film overlaps the cover insulating film 2. However, the manufacturing process of etching the TiNiAg film 3 having the above-mentioned film thickness is very difficult process with respect to workability or technology, and also manufacturing costs become high.

[0004]

With reference to Figs. 10(a)-(e), an explanation will be made on a manufacturing method for solving such problems. In the first process, a cover insulating film 2 made of a PSG film having a thickness of, for example, 10000 angstroms is formed on an aluminum film 1 by using an atmospheric pressure CVD method, as illustrated in Fig. 10(a) which shows a condition after finishing the first process.

[0005]

In the second process, after finishing the first process, the cover insulating film 2 is masked by a photo resist pattern 4 which is formed on the cover insulating film 2 by using a photolithography method and which has an opening at a location corresponding to a bonding pad electrode, as illustrated in Fig. 10(b) which shows a condition after finishing the second process.

[0006]

After finishing the second process, in the third process, by using the photo resist pattern 4 as an etching mask, a portion of the cover insulating film 2 at a location corresponding to the bonding pad electrode is removed by using an isotropic etching method, for example, a wet etching method. Thereby, an opening is formed in the cover insulating film 102, as illustrated by Fig. 10(c) which shows a condition after finishing the third process.

[0007]

After finishing the third process, in the fourth process, while leaving the photo resist pattern 4, a TiNiAg film 3 is formed on the photo resist pattern 4 by using a sputtering method, as illustrated in Fig. 10(d) which shows a condition after finishing the fourth process.

[0008]

After finishing the fourth process, in the fifth process, portions of the TiNiAg film 3 on the photo resist pattern 4 are removed by using a lift-off method, and further the photo resist pattern 4 is removed, as illustrated in Fig. 10(e) which shows a condition after finishing the fifth process.

[0009]

[Problems to be Solved by the Invention]

When the bonding pad electrode is fabricated by using the above-mentioned method illustrated in Figs. 10, there occurs the following problem. That is, as shown in Fig. 10(c), the cover insulating film 2 is side-etched wider than the opening of the photo resist pattern 4, and, as shown in Fig. 10(d), on the aluminum film 1, a gap is produced between the TiNiAg film 3 and the cover insulating film 2. Thus, as shown in Fig. 10(e), a bonding pad electrode structure is produced in which the aluminum film 1 is exposed via the gap between the TiNiAg film 3 and the cover insulating film 2. In such bonding pad electrode structure, it is impossible completely protect the aluminum film 1 from the corrosive substance. Also, in order to prevent the cover insulating film 2 from being side-etched wider than the opening of the photo resist pattern 4, it is conceivable to ion-etch, such as plasma-etch, a portion of the cover insulating film 2 corresponding to a pad location, by using the photo resist pattern 4 as an etching mask. However, in this case, there is a possibility that a portion of the TiNiAg film 3 on the photo resist pattern 4 connects with a portion of

the TiNiAg film 3 on the aluminum film 1. Thereby, it becomes difficult to remove portions of the TiNiAg film 3 on the photo resist pattern 4 by using a lift-off method.

The present invention is thought out taking the above-mentioned problems into consideration, and it is an object of the present invention to provide a semiconductor device having a bonding pad electrode which can be formed by using a lift-off method and in which a lower electrode layer is not exposed between a cover insulating film and an upper metal layer, and to provide a method of manufacturing such semiconductor device.

[0010]

[Means to Solve the Problems]

(1) The semiconductor device according to the present invention is characterized in that, in a semiconductor device in which a bonding pad electrode is formed by stacking a cover insulating film on a lower metal layer, by forming an opening in said cover insulating film to expose said lower metal layer and by covering the exposed lower metal layer with an upper electrode layer made of material having corrosion resistance against substance which is corrosive to said lower electrode layer, a step portion is provided in said cover insulating film by making the size of an upside portion of said opening of said cover insulating film larger than the size of a down side portion of said opening, and said upper electrode layer overlaps a step surface of said step portion.

(2) The semiconductor device according to the present invention is characterized in that, in the semiconductor device as set forth in the above item (1), said cover insulating film comprises a lower layer silicon nitride film and an upper layer PSG film, and said step surface is a surface of said silicon nitride film.

(3) The semiconductor device according to the present invention is characterized in that, in the semiconductor device as set forth in the above item (1), said cover insulating film comprises a PSG film.

(4) The semiconductor device according to the present invention is characterized in that, in the semiconductor device as set forth in any one of the above items (1)-(3), said lower electrode layer comprises a metal film of aluminum system, and said upper electrode layer comprises a metal film which has corrosion resistance against substance corrosive to aluminum.

(5) The semiconductor device according to the present invention is characterized in that, in the semiconductor device as set forth in the above item (4), said upper electrode layer comprises a TiNiAg film.

(6) The semiconductor device according to the present invention is characterized in that, in the semiconductor device as set forth in the above item (4) or (5), a high conductivity metal plate is coupled onto said bonding pad electrode via a conductive paste.

(7) The semiconductor device according to the present invention is characterized in that, in the semiconductor device as set forth in the above item (6), said conductive paste is an Ag paste, and said high conductivity metal plate is a copper plate.

(8) The semiconductor device according to the present invention is characterized in that, in the semiconductor device as set forth in the above item (6) or (7), said bonding pad electrode is a source pad electrode of a power MOSFET.

(9) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in a method of manufacturing a semiconductor device in which a bonding pad electrode is formed by stacking a cover insulating film on a lower metal layer, by forming an opening in said cover insulating film to expose said lower metal layer and by covering the exposed lower metal layer with an upper electrode layer made of material having corrosion resistance against substance which is corrosive to said lower electrode layer, a step portion is provided in said cover insulating film by making the size of an upside portion of said opening of said cover insulating film larger than the size of a down side portion of said opening, and said upper electrode layer is formed such that said upper electrode layer overlaps a step surface of said step portion.

(10) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in the above item (9), forming said step portion is performed by side-etching said cover insulating film by isotropically etching said cover insulating film by using a photo resist pattern as a mask, and forming said upper electrode layer is performed by using a lift-off method in which said photo resist pattern is

used as a mask.

(11) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in the above item (10), as said cover insulating film, a lower layer silicon nitride film and an upper layer PSG film are stacked, said side-etching is performed on said PSG film, thereafter said silicon nitride film is plasma etched by using said photo resist pattern as a mask, thereby exposing via said PSG film a surface of said silicon nitride film as said step surface, wherein said upper layer electrode layer is formed thereon, thereafter the upper layer electrode layer on said photo resist pattern is removed by using said lift-off method, thereby said upper layer electrode layer is left unremoved on the portion of said lower electrode layer exposed by said opening of said PSG film and of said silicon nitride and on said step surface.

(12) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in the above item (10), as said cover insulating film, a lower layer silicon nitride film is stacked, said silicon nitride film is plasma etched by using a first photo resist pattern as a mask, thereby an opening of said silicon nitride film is formed which exposes said lower layer electrode layer, wherein, after removing said first photo resist pattern, a PSG film is formed thereon, said side-etching is performed on said PSG film by using a second photo resist pattern having an opening wider than the opening of said silicon nitride film as said photo resist pattern, thereby a surface of said silicon nitride film exposed via said PSG film becoming said step surface, wherein said upper layer electrode layer is formed thereon, thereafter the upper layer electrode layer on said second photo resist pattern is removed by using said lift-off method, thereby said upper layer electrode layer is left unremoved on the portion of said lower electrode layer exposed by said opening of said PSG film and of said silicon nitride and on said step surface.

(13) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in the above item (10), as said cover insulating film, a PSG film is stacked, said PSG film is

anisotropically or isotropically etched by using a first photo resist pattern having an opening of a predetermined width as a mask, thereby a trench is formed in said PSG film, said PSG film is further isotropically etched by using a second photo resist pattern having an opening wider than the opening of said trench as a mask until said lower layer electrode layer is exposed from said trench, thereby forming said step surface at an end portion of the opening of said PSG film, wherein a film constituting said upper layer electrode layer is formed thereon, thereafter the upper layer electrode layer on said second photo resist pattern is removed by using said lift-off method, thereby said upper layer electrode layer is left unremoved on the portion of said lower electrode layer exposed by said opening of said PSG film and on said step surface.

(14) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in any one of the above items (9)-(13), said lower electrode layer comprises a metal film of aluminum system, and said upper electrode layer comprises a metal film which has corrosion resistance against substance corrosive to aluminum.

(15) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in the above item (14), said upper electrode layer comprises a TiNiAg film.

(16) The method of manufacturing a semiconductor device according to the present invention is characterized in that the method of manufacturing a semiconductor device as set forth in the above item (14) or (15) further comprises coupling a high conductivity metal plate onto said bonding pad electrode via a conductive paste.

(17) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in the above item (16), said conductive paste is an Ag paste, and said high conductivity metal plate is a copper plate.

(18) The method of manufacturing a semiconductor device according to the present invention is characterized in that, in the method of manufacturing a semiconductor device as set forth in the above item (16) or

(17), said bonding pad electrode is a source pad electrode of a power MOSFET.

[0011]

[Mode for Carrying Out the Invention]

With reference to Fig. 1, an explanation will now be made on a MOSFET 100 having a UMOS structure according to a first embodiment of the present invention. A reference numeral 11 designates an N^+ type silicon substrate having a conductivity type and having a high impurity concentration. On the silicon substrate 11, an N^- type epitaxial layer 12 is stacked. A U-shaped trench 13 is formed in cell portion A at the surface of the epitaxial layer 12. Inside the U-shaped trench 13, a gate electrode 14 made of polysilicon is buried and formed via a gate oxide film not shown in the drawing. At a surface layer of the epitaxial layer 14 separated by the U-shaped trench 13 of the cell portion A, there is formed a P type base region 15 having another conductivity type. At a surface layer of the base region 15 and in contact with the U-shaped trench 13, there is formed an N^+ type source region 16. In a gate finger portion B interposed between the cell portion A and the cell portion A on the epitaxial layer 12, a polysilicon gate finger 18 is formed via a field oxide film 17, which polysilicon gate finger 18 is formed simultaneously with the gate electrode 14. On the epitaxial layer 12 on which the structure mentioned above is formed, an interlayer insulating film 19 comprising a BPSG film is formed. On the interlayer insulating film 19, there is formed a source electrode 20 which is electrically contacted with the base region 15 and the source region 16 in the cell portion A via openings of the interlayer insulating film 19 and which comprises an aluminum film as a lower electrode layer. In the gate finger portion B, there is formed an aluminum gate finger 21 which is electrically contacted with the polysilicon gate finger 18 and which is formed simultaneously with the source electrode 20. On such structure, a silicon nitride film 22a and a PSG film 22b are formed in order as a cover insulating film 22. Via openings of the silicon nitride film 22a and the PSG film 22b, there is formed a TiNiAg film 23 in a source pad portion C on the source electrode 20. The opening of the PSG film 22b is wider than the opening of the silicon nitride film 22a, and there is produced a step portion at an edge of the opening of the cover insulating film 22. That is,

a step surface 22c is formed by a surface portion of the silicon nitride film 22a which is exposed via the opening of the PSG film 22b. The TiNiAg film 23 is formed such that the TiNiAg film 23 overlaps the step surface 22c. The cross sectional view shown in Fig. 1 shows a cross section taken along the line X-X of the chip surface of MOSFET shown in Fig. 2. In Fig. 2, a reference symbol D designates a gate pad portion.

[0012]

In the above-mentioned structure, the cover insulating film 22 comprises the silicon nitride film 22a and the PSG film 22b. The opening of the PSG film 22b is wider than the opening of the silicon nitride film 22a, and there is produced a step portion at an edge of the opening as the cover insulating film 22. The TiNiAg film 23 is formed such that the TiNiAg film 23 overlaps the step surface 22c formed by the silicon nitride film 22a exposed via the PSG film 22b. Therefore, it is possible to protect the source electrode 20 made of an aluminum film of the source pad portion C from the corrosive substance.

[0013]

Next, with reference to Figs. 3(a)-(f), an explanation will be made on a method of manufacturing the MOSFET 100, according to a first embodiment. A process until the source electrode 20 and the aluminum gate finger 21 are formed can be the same as a conventional process, and an explanation thereof will be omitted here. Therefore, a process of forming the cover insulating film 22 and a process thereafter will be described here, by using drawings which show only cross sections corresponding to a portion on the source electrode 20 and in the proximity of an edge of the opening of the cover insulating film. First, in the first process, as shown in Fig. 3(a) which shows a condition after finishing this process, a silicon nitride film 22a having a film thickness of, for example, 5000 angstroms and a PSG film 22b having a film thickness of, for example, 10000 angstroms are sequentially stacked as a cover insulating film 22 on a source electrode 20. The silicon nitride film 22a is formed by using a plasma CVD method, and the PSG film 22b is formed by using an atmospheric pressure CVD method.

[0014]

After finishing the first process, in the second process, as shown in Fig.

3(b) which shows a condition after finishing the second process, a photo resist film having predetermined patterns, i.e., a photo resist pattern 25 is formed on the PSG film 22b as a mask by using a photolithography method. The photo resist pattern 25 has an opening at a source pad portion C.

[0015]

After finishing the second process, in the third process, as shown in Fig. 3(c) which shows a condition after finishing the third process, while leaving the photo resist pattern 25, and by using the photo resist pattern 25 as an etching mask, a portion of the PSG film 22b at the source pad portion C is removed by isotropic etching, for example, by an wet etching method. Thereby, an opening 52b is formed in the PSG film 22b. In this process, the PSG film 22b is side-etched with respect to the photo resist pattern 25, and the opening of the PSG film 22b becomes wider than the opening of the photo resist pattern 25 by the amount of the side-etching.

[0016]

After finishing the third process, in the fourth process, as shown in Fig. 3(d) which shows a condition after finishing the fourth process, by using the photo resist pattern 25 as an etching mask, a portion of the silicon nitride film 22a corresponding to the source pad portion C is removed by plasma etching. Thereby, an opening is formed in the silicon nitride film 22a. In this case, the width of the opening of the silicon nitride film 22a becomes approximately the same as that of the opening of the patterned photo resist film 25. Therefore, the opening of the PSG film 22b becomes wider than the opening of the silicon nitride film 22a, and there is produced a step portion at each edge of the opening of the cover insulating film 22. That is, the step surface 22c is formed by a surface portion of the silicon nitride film 22a which is exposed via the PSG film 22b.

[0017]

After finishing the fourth process, in the fifth process, as shown in Fig. 3(e) which shows a condition after finishing the fifth process, while leaving the photo resist pattern 25, an TiNiAg film 23 is deposited by using a sputtering method or a vapor deposition method. The TiNiAg film 23 comprises, for example, a Ti film having a thickness of 1000 angstroms, an Ni film having a thickness of 1000 angstroms and an Ag film having a thickness of 10000 angstroms. In this case, the TiNiAg film 23 is formed

such that a portion of the TiNiAg film 23 overlaps the exposed step surface 22c at each edge portion of the opening of the cover insulating film 22. Here, a portion of the TiNiAg film 23 deposited on the photo resist pattern 25 and a portion of the TiNiAg film 23 deposited on the source electrode 20 and the step surface 22c do not connect with each other.

[0018]

After finishing the fifth process, in the sixth process, as shown in Fig. 3(f) which shows a condition after finishing the sixth process, a portion of the TiNiAg film 23 on the photo resist pattern 25 is removed by using a lift-off method, and further the photo resist pattern 25 is removed.

[0019]

In the above-mentioned manufacturing method, the silicon nitride film 22a and the PSG film 22b are formed in order as the cover insulating film 22. By using the photo resist pattern 25, the side-etching which is caused by the isotropical etching method is performed, thereby the opening of the PSG film 22b is formed wider than the opening of the silicon nitride film 22a formed by plasma etching. Therefore, there is produced a step portion at each edge of the opening of the cover insulating film 22, and the step surface 22c is formed by a surface portion of the silicon nitride film 22a which is exposed via the PSG film 22b. By using a lift-off method, the TiNiAg film 23 is formed such that the TiNiAg film 23 overlaps the step surface 22c. Therefore, it is possible to protect the source electrode 20 made of an aluminum film of the source pad portion C from the corrosive substance.

[0020]

Next, with reference to Figs. 4(a)-(f), an explanation will be made on a method of manufacturing the MOSFET 100, according to a second embodiment. First, in the first process of the second embodiment, as shown in Fig. 4(a) which shows a condition after finishing the first process, a silicon nitride film 22a is stacked as the lower layer of a cover insulating film 22 on a source electrode 20 by using a plasma CVD method. The silicon nitride film 22a has a thickness, for example, of 5000 angstroms.

[0021]

After finishing the first process, in the second process, as shown in Fig. 4(b) which shows a condition after finishing the second process, a photo

resist pattern 25a is formed on the silicon nitride film 22a by using a photolithography method. The photo resist pattern 25a has an opening at a source pad portion C. Then, by using the photo resist pattern 25a as an etching mask, a portion of the silicon nitride film 22a at the source pad portion C is removed by using plasma etching. Thereby, an opening is formed in the silicon nitride film 22a.

[0022]

After finishing the second process, in the third process, as shown in Fig. 4(c) which shows a condition after finishing the third process, the patterned photo resist film 25a is removed. Thereafter, a PSG film 22b is formed as the upper layer of the cover insulating film 22 on the silicon nitride film 22a having the opening, by using an atmospheric pressure CVD method. The PSG film 22b has a thickness of, for example, 10000 angstroms.

[0023]

After finishing the third process, in the fourth process, as shown in Fig. 4(d) which shows a condition after finishing the fourth process, a photo resist film 25b is formed on the PSG film 22b as a mask by using a photolithography method. The photo resist pattern 25b has an opening at the source pad portion C which is wider than the opening of the silicon nitride film 22a. Then, by using the photo resist pattern 25b as an etching mask, a portion of the PSG film 22b at the source pad portion C is removed by an isotropic etching method, for example, by using a wet etching method. Thereby, an opening is formed in the PSG film 22b. In this process, the PSG film 22b is side-etched with respect to the photo resist pattern 25b, and the opening of the PSG film 22b becomes wider than the opening of the photo resist pattern 25b by the amount of the side-etching. Thus, the opening of the PSG film 22b becomes wider than the opening of the silicon nitride film 22a. Thereby, there is produced a step portion at each edge of the opening of the cover insulating film 22, and the step surface 22c is formed by a surface portion of the silicon nitride film 22a which is exposed via the PSG film 22b.

[0024]

After finishing the fourth process, in the fifth process, as shown in Fig. 4(e) which shows a condition after finishing the fifth process, while leaving the photo resist pattern 25b, an TiNiAg film 23 is deposited thereon by

using a sputtering method or a vapor deposition method. The TiNiAg film 23 comprises, for example, a Ti film having a thickness of 1000 angstroms, an Ni film having a thickness of 1000 angstroms and an Ag film having a thickness of 10000 angstroms. The TiNiAg film 23 is formed such that the TiNiAg film 23 overlaps the step surface 22c exposed at the edge portion of the opening of the cover insulating film 22. In the first embodiment, the width of the opening of the silicon nitride film 22a and the width of the opening of the photo resist pattern 25 are the same as each other. However, in this embodiment, the opening of the photo resist pattern 25b is made wider than the opening of the silicon nitride film 22a. Therefore, the size of a portion of the TiNiAg film 23 which overlaps the step surface 22c becomes larger than that of the first embodiment. In this case, a portion of the TiNiAg film 23 deposited on the patterned photo resist film 25b and a portion of the TiNiAg film 23 deposited on the source electrode 20 and the step surface 22c do not connect with each other.

[0025]

After finishing the fifth process, in the sixth process, as shown in Fig. 4(f) which shows a condition after finishing the sixth process, a portion of the TiNiAg film 23 on the photo resist pattern 25b is removed by using a lift-off method, and further the photo resist pattern 25b is removed.

[0026]

In the above-mentioned manufacturing method, first, the silicon nitride film 22a is formed as the cover insulating film 22. Then, by using the patterned photo resist film 25a, an opening is formed in the silicon nitride film 22a by using plasma etching. Thereafter, the PSG film 22b is stacked. By using the patterned photo resist film 25b which has an opening wider than the opening of the silicon nitride film 22a, an opening is formed in the PSG film 22b by using the side-etching provided by an isotropical etching method. The opening of the PSG film 22b becomes wider than the opening of the patterned photo resist film 25b. Therefore, there is produced a step portion at an edge of the opening of the cover insulating film 22, and the step surface 22c is formed by a surface portion of the silicon nitride film 22a which is exposed via the PSG film 22b. By using a lift-off method, the TiNiAg film 23 is formed such that the TiNiAg film 23 overlaps the step surface 22c and such that the size of a portion of the

TiNiAg film 23 which overlaps the step surface 22c becomes larger than that of the first embodiment. Therefore, in this embodiment, it is possible to protect the source electrode 20 made of an aluminum film of the source pad portion C from the corrosive substance with a margin larger than that of the first embodiment.

[0027]

With reference to Fig. 5, an explanation will now be made on a MOSFET 200 having an UMOS structure according to a second embodiment of the present invention. In the MOSFET 200, a structure from the N^+ type silicon substrate 11 to the source electrode 20 and the aluminum gate finger 21 is the same as that of the MOSFET 100, and an explanation concerning these portions is omitted here. Here, an explanation will be made on a structure of portions on the source electrode 20 and the aluminum gate finger 21. In the MOSFET 200, a cover insulating film 32 is formed on the source electrode 20 and the aluminum gate finger 21. The cover insulating film 32 is made of a PSG film. A TiNiAg film 33 is formed at the source pad portion C on the source electrode 20 via an opening of the cover insulating film 32. There is provided a step portion at an end portion of the opening of the cover insulating film 32. The TiNiAg film 33 is formed such that the TiNiAg film 33 overlaps a step surface 32a of the step portion. The cross sectional view shown in Fig. 5 shows a cross section of a portion similar to the portion taken along the section line X-X of the chip surface of MOSFET 100 shown in Fig. 2.

[0028]

In the above-mentioned structure, the step portion is formed at the end portion of the opening of the cover insulating film 32 made of a PSG film. Also, the TiNiAg film 33 is formed such that the TiNiAg film 33 overlaps the step surface 32a of the step portion. Therefore, it is possible to protect the source electrode 20 made of an aluminum film of the source pad portion C from the corrosive substance.

[0029]

Next, with reference to Figs. 6(a)-(f), an explanation will be made on an embodiment of a method of manufacturing the MOSFET 200. A process until fabrication of the source electrode 20 and the aluminum gate

finger 21 can be done by using a conventionally used technology, and an explanation thereof is omitted here. Therefore, a process of forming the cover insulating film 32 and a process thereafter will be described only with reference to cross sections of a portion on the source electrode 20 and in the proximity of an end portion of the opening of the cover insulating film.

In the first process, as shown in Fig. 6(a) which shows a condition after finishing this process, a cover insulating film 32 is formed on a source electrode 20 by using a plasma CVD method. The cover insulating film 32 is made, for example, of a PSG film which has a thickness of 15000 angstroms.

[0030]

After finishing the first process, in the second process, as shown in Fig. 6(b) which shows a condition after finishing this process, a photo resist pattern 35a is formed on the cover insulating film 32 by using a photolithography method. The photo resist pattern 35a has an opening at a source pad portion C.

[0031]

After finishing the second process, in the third process, as shown in Fig. 6(c) which shows a condition after finishing this process, by using the photo resist pattern 35a as an etching mask, a portion of the cover insulating film 32 corresponding to the source pad portion C is removed by using an isotropic etching method, for example, a wet etching, or an anisotropic etching method, for example, an ion etching of a plasma etching. (In the embodiment of Fig. 6(c), by using the isotropic etching), the cover insulating film 32 is removed such that the thickness of the cover insulating film 32 becomes, for example, 7500 angstroms to form a trench 32b. In this case, a portion of the cover insulating film 32 just under the photo resist film pattern 35a is side-etched with respect to the photo resist pattern 35a. Therefore, the size of the opening of the trench 32b of the cover insulating film 32 becomes wider than the width of the opening of the photo resist pattern 35a by the amount of the side etch.

[0032]

After finishing the third process, in the fourth process, as shown in Fig. 6(d) which shows a condition after finishing this process, the photo resist pattern 35a is removed, and the cover insulating film 32 is newly masked

by a photo resist pattern 35b which has an opening at the source pad portion C, the opening of the photo resist pattern 35b being wider than the opening of the trench 32b of the cover insulating film 32. Then, a portion of the cover insulating film 32 exposed via the opening of the patterned photo resist film 35b is removed by an isotropic etching method, for example, a wet etching method, until a portion of the source electrode 20 is exposed via the trench 32b of the cover insulating film 32. Thereby, an opening 32c is formed in the cover insulating film 32. In this case, a portion of the cover insulating film 32 just under the patterned photo resist film 35b is side-etched with respect to the photo resist pattern 35b, and a step portion is produced at an end portion of the opening of the cover insulating film 32. Thereby, a step surface 32a of the cover insulating film 32 is formed.

[0033]

After finishing the fourth process, in the fifth process, as shown in Fig. 6(e) which shows a condition after finishing this process, while leaving the patterned photo resist film 35b, an TiNiAg film 33 is deposited by using a sputtering method or a vapor deposition method. The TiNiAg film 33 comprises, for example, a Ti film having a thickness of 1000 angstroms, an Ni film having a thickness of 1000 angstroms and an Ag film having a thickness of 10000 angstroms. In this case, the TiNiAg film 33 is formed such that a portion of the TiNiAg film 33 overlaps the step surface 32a exposed at an end portion of the opening of the cover insulating film 32. In the manufacturing method of the above-mentioned MOSFET 100 according to the first embodiment, the width of the opening of the silicon nitride film 22a and the width of the opening of the patterned photo resist film 25 are the same as each other. However, in this embodiment, the opening of the patterned photo resist film 35b is wider than the opening of the cover insulating film 32. Therefore, the size of overlapping with the step surface 32a at the end portion of the cover insulating film 32 becomes larger than that of the first embodiment of the manufacturing method of the MOSFET 100. In this case, a portion of the TiNiAg film 33 on the photo resist pattern 35b and a portion of the TiNiAg film 33 on the source electrode 20 and the step surface 32a do not connect with each other.

[0034]

After finishing the fifth process, in the sixth process, as shown in Fig.

6(f) which shows a condition after finishing this process, a portion of the TiNiAg film 33 on the photo resist pattern 35b is removed by using a lift-off method, and further the photo resist pattern 35b is removed.

[0035]

In the above-mentioned manufacturing method, the cover insulating film 32 made of a PSG film is formed. By using the photo resist pattern 35a as an etching mask, a trench 32b is formed in the cover insulating film 32 by using an isotropic etching method or an anisotropic etching method. By using a photo resist pattern 35b which has an opening wider than the opening of the trench 32b of the cover insulating film 32, the cover insulating film 32 is removed by isotropic etching, until a portion of the source electrode 20 is exposed via the trench 32b of the cover insulating film 32. Thereby, an opening 32c is formed in the cover insulating film 32. In this case, the cover insulating film 32 just under the photo resist pattern 35b is side-etched. Therefore, there is produced a step portion at an end portion of the opening of the cover insulating film 32, and thereby the exposed step surface 32a is formed. The TiNiAg film 33 is formed by using a lift-off method such that a portion of the TiNiAg film 33 overlaps the step surface 32a and the size of a portion of the TiNiAg film 33 which overlaps the step surface 32a becomes larger than that of the first embodiment concerning the MOSFET 100. Therefore, it is possible to protect the source electrode 20 made of an aluminum film of the source pad portion C from the corrosive substance with a margin larger than that of the first embodiment concerning the MOSFET 100.

[0036]

An explanation will now be made on an electrode extracting structure used when the above-mentioned MOSFET 100 and MOSFET 200 are packaged. Here, as an example, such electrode extracting structure for the MOSFET 100 is explained with reference to Fig. 7 and Fig. 8. Description of the MOSFET 100 was already provided in the above and is not repeated here. As shown in Figs. 7 and 8, the TiNiAg film 23 of the MOSFET 100 is coupled with a high conductivity metal plate 52 for electrode extraction to an external terminal via a conductive paste 51, for example, Ag paste. The high conductivity metal plate 52 is, for example, a copper plate. By providing the MOSFET 100 with the above-mentioned electrode extracting

structure, it is possible to protect the source electrode 20 from corrosive substance such as chlorine and the like contained in the Ag paste. Also, it is possible to reduce an electrical resistance from the source electrode 20 to the external terminal. Therefore, it is possible to reduce on-resistance of the packaged MOSFET.

[0037]

In the above, description was made on MOSFET's having a UMOS structure. However, the present invention is not limited to such device. The present invention can be applied to a MOSFET having a gate planar structure, and can be applied to devices other than MOSFET. Also, with respect to the electrode extracting structure, it is preferable to use such structure in a power device, because it is possible to reduce an operation resistance thereof by using such structure.

[0038]

[Effect of the Invention]

According to the semiconductor device and the method of manufacturing such semiconductor device of the present invention, in order to protect a lower metal layer constituting a bonding pad electrode from the corrosive substance, a cover insulating film is formed on the lower metal layer, and an opening is formed in the cover insulating film to expose the lower metal layer. When, on the exposed lower metal layer, an upper electrode layer having corrosion resistance against the substance that may corrode the lower metal layer is formed, the upper portion of the opening of the cover insulating film is made wider than the lower portion thereof such that a step portion is provided. Also, the upper metal layer is formed on the step surface of the step portion such that the upper metal layer overlaps the step surface. Therefore, it is possible to manufacture a bonding pad electrode in which the lower metal layer is not exposed between the cover insulating film and the upper metal layer, with good workability and technically easily. Also, it is possible to manufacture a semiconductor device in which the lower metal layer can be completely protected from the corrosive substance, at low cost.

Also, by coupling a high conductivity metal plate to the upper metal layer via conductive paste, it is possible to reduce an electrical resistance to an external terminal, while protecting the lower metal layer from a

corrosive substance such as chlorine and the like contained in the conductive paste, and to reduce an operation resistance of the packaged semiconductor device.

[Brief Description of drawings]

[Fig. 1]

Fig. 1 is a cross sectional view showing a main portion of a MOSFET according to a first embodiment of the present invention.

[Fig. 2]

Fig. 2 is a schematic plan view of a pattern of the MOSFET of Fig. 1.

[Fig. 3]

Figs. 3 are cross sectional views of main portions illustrating a manufacturing process of the MOSFET of Fig. 1 according to a first embodiment.

[Fig. 4]

Figs. 4 are cross sectional views of main portions illustrating a manufacturing process of the MOSFET of Fig. 1 according to a second embodiment.

[Fig. 5]

Fig. 5 is a cross sectional view showing a main portion of a MOSFET according to a second embodiment of the present invention.

[Fig. 6]

Figs. 6 are cross sectional views of main portions illustrating a manufacturing process of the MOSFET of Fig. 5 according to an embodiment.

[Fig. 7]

Fig. 7 is a cross sectional view showing a main portion of an electrode extracting structure to an external terminal used in the MOSFET of Fig. 1.

[Fig. 8]

Fig. 8 is a schematic plan view of a pattern of the electrode extracting structure of Fig. 7.

[Fig. 9]

Fig. 9 is a cross sectional view showing a main portion of a conventional bonding pad structure.

[Fig. 10]

Figs. 10 are cross sectional views of a main portion illustrating

problems when the bonding pad electrode shown in Fig. 9 is manufactured by using a lift-off method.

[Explanations of Letters or Numerals]

C a source pad portion

20 a source electrode (a lower electrode layer)

22, 32 cover insulating films

22a a silicon nitride film

22b a PSG film

22c, 32a step surfaces

32b a trench of a cover insulating film

32c an opening of a cover insulating film

23, 33 TiNiAg films (upper electrode layers)

25 a photo resist pattern

25a, 35a first photo resist patterns

25b, 35b second photo resist patterns

51 conductive paste (Ag past)

52 a high conductivity metal plate (a copper plate)

100, 200 MOSFET's

[Document's Name] Abstract

[Abstract]

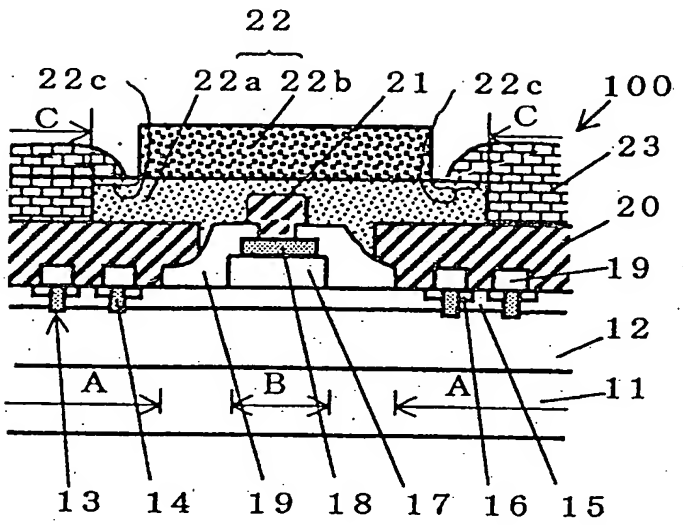
[Problems to be Solved by the Invention] When a TiNiAg film is formed on a source electrode via an opening of a cover insulating film by using a lift-off method in order to protect the source electrode from being corroded by corrosive substance via the opening of the cover insulating film for forming a bonding pad, there is a problem that the source electrode is exposed between the cover insulating film and the TiNiAg film.

[Means to solve the Problems] A silicon nitride film 22a and a PSG film 22b are formed in order as a cover insulating film 22. A TiNiAg film 23 is formed on a source electrode 20 via an opening of the silicon nitride film 22a and the PSG film 22b. The opening of the PSG film 22b is formed wider than the opening of the silicon nitride film 22a. Therefore, there is produced a step portion at an edge portion of the opening of the cover insulating film 22, and the step surface 22c is formed by a surface portion of the silicon nitride film 22a which is exposed via the PSG film 22b. By using a lift-off method, the TiNiAg film 23 is formed such that the TiNiAg film 23 overlaps the step surface 22c.

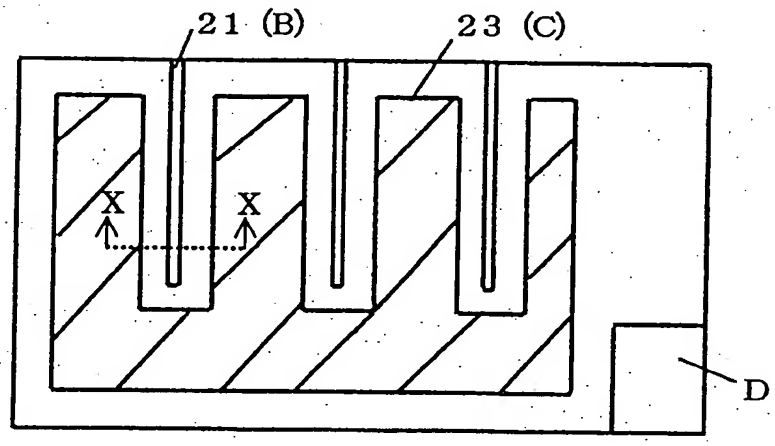
[Chosen Drawing] Fig. 1

[Name of Document] [Drawings]

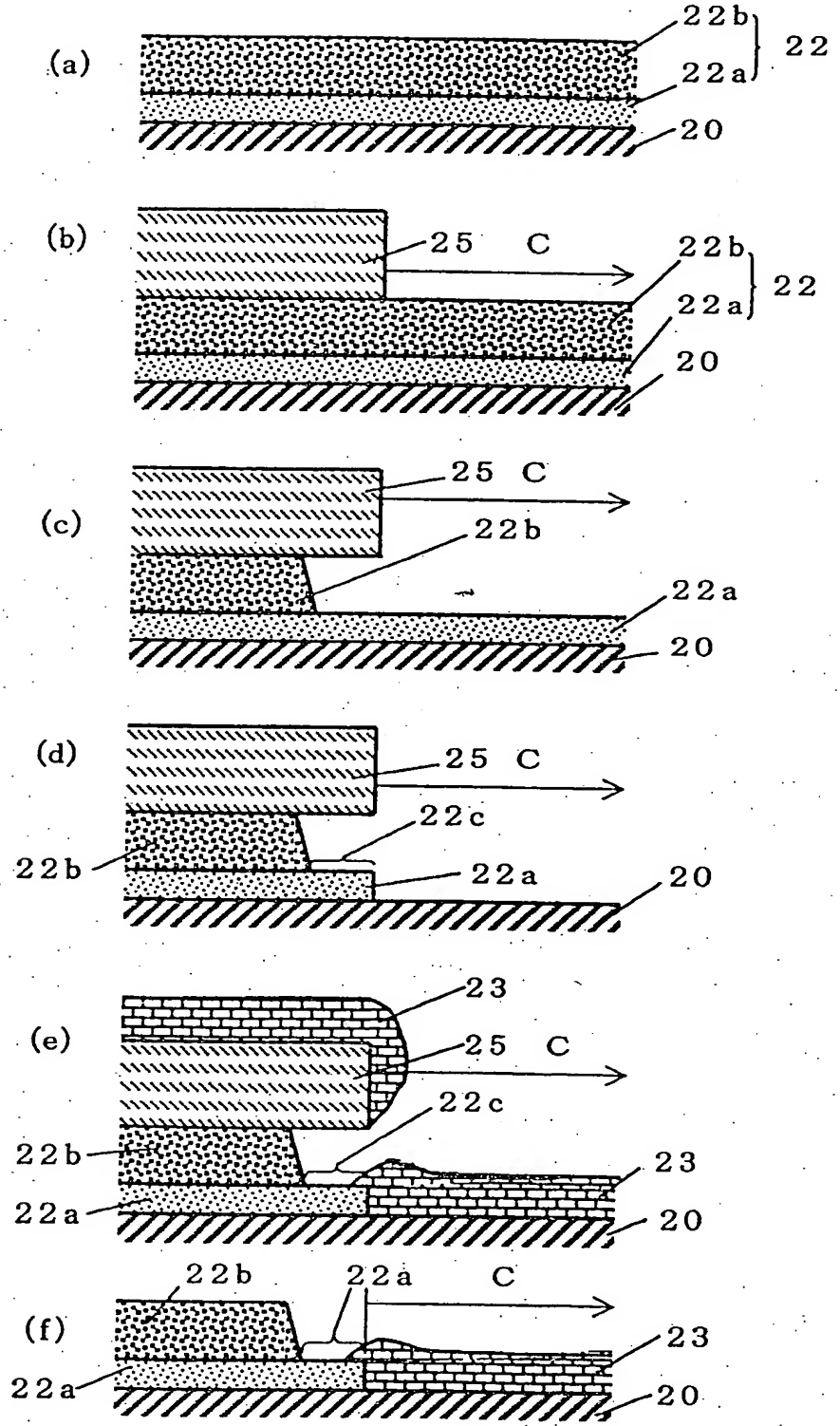
[Fig. 1]



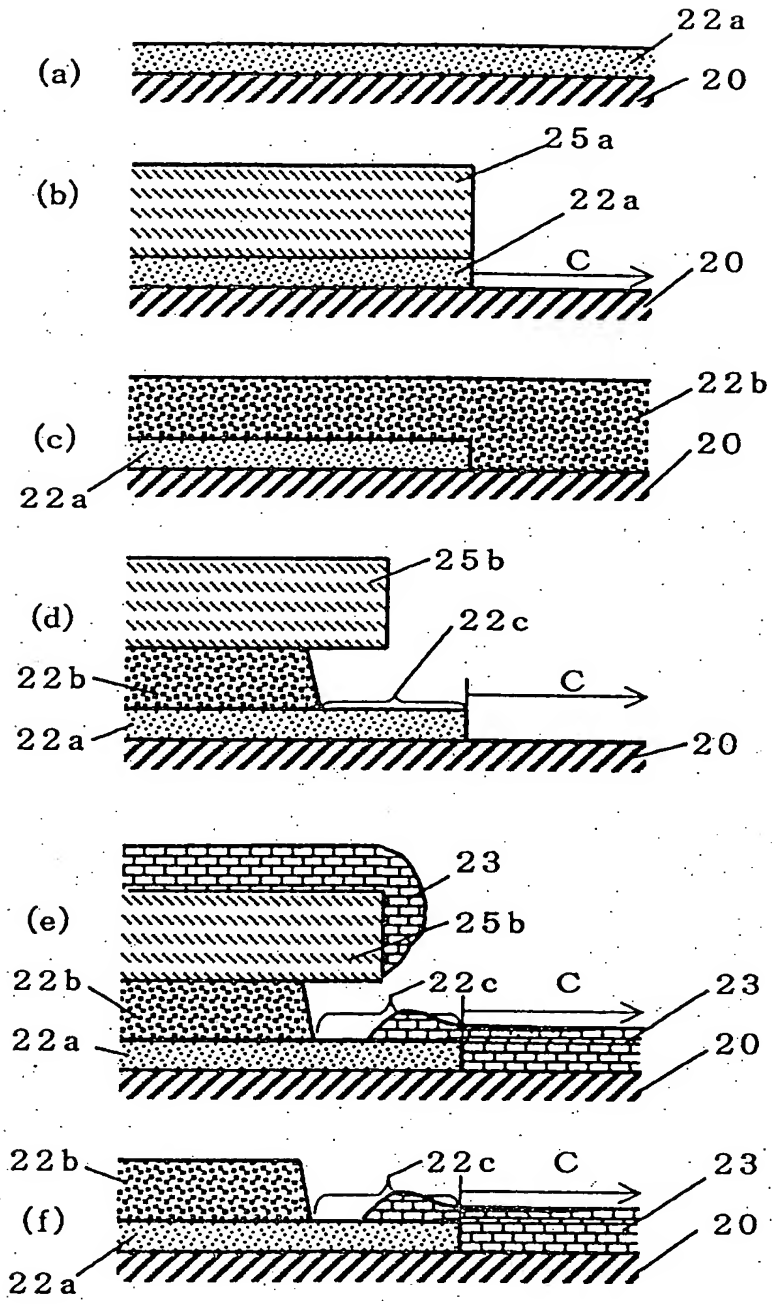
[Fig. 2]



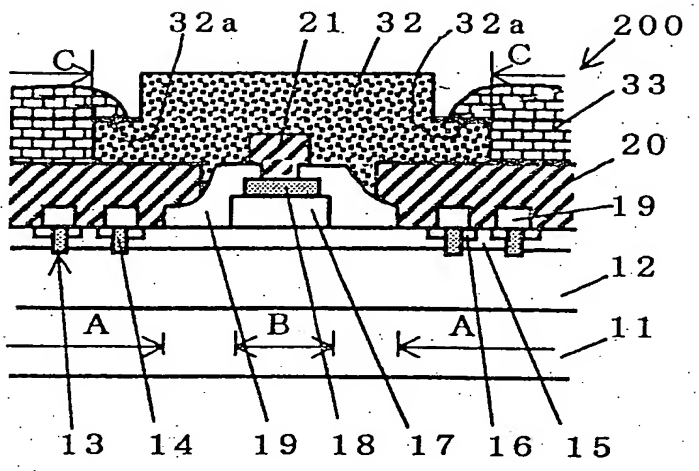
[Fig. 3]



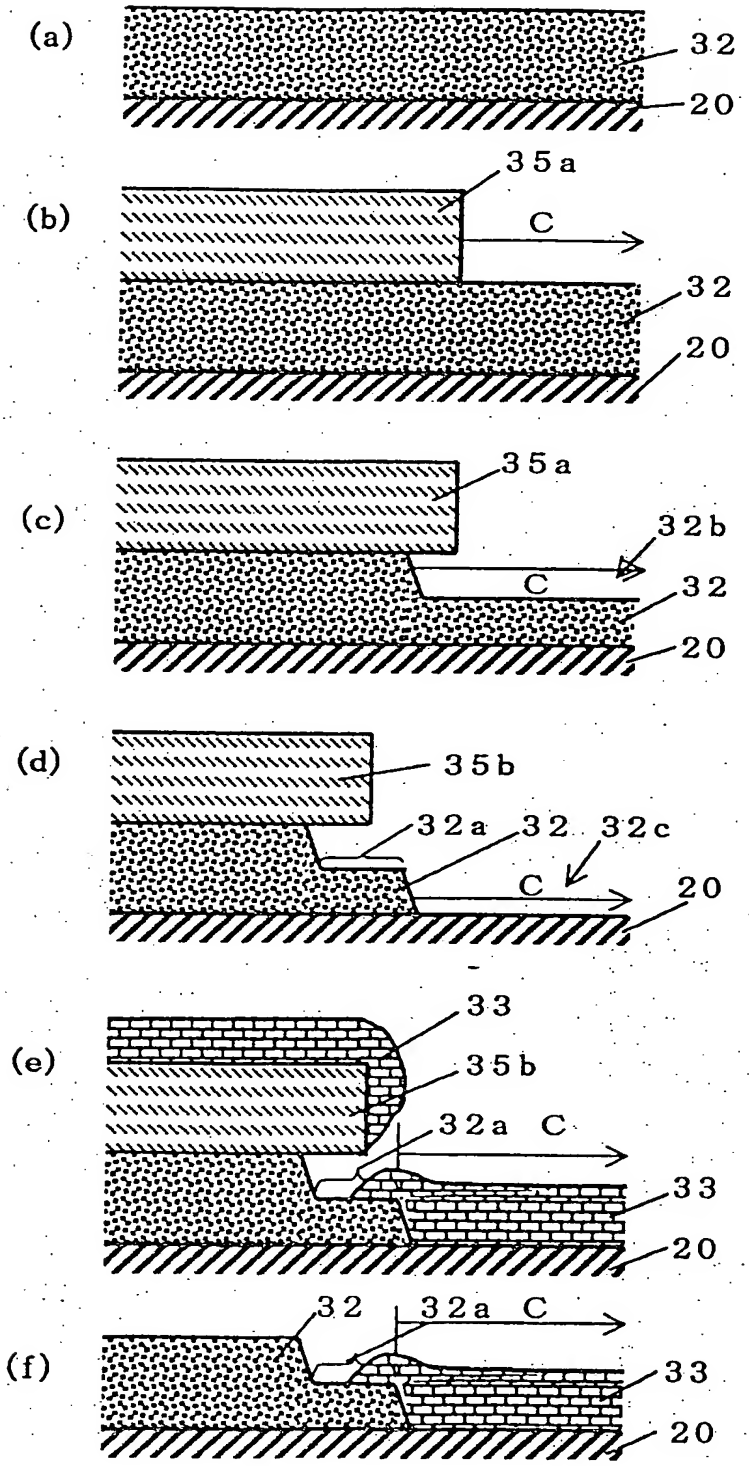
[Fig. 4]



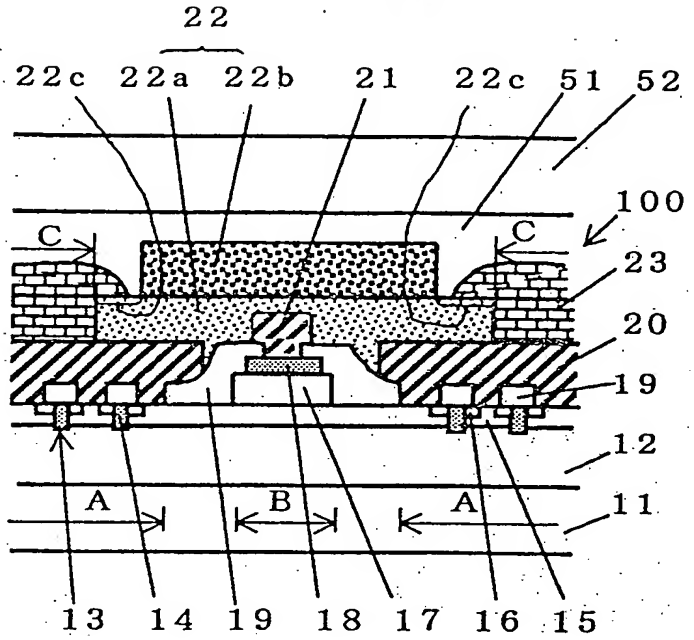
[Fig. 5]



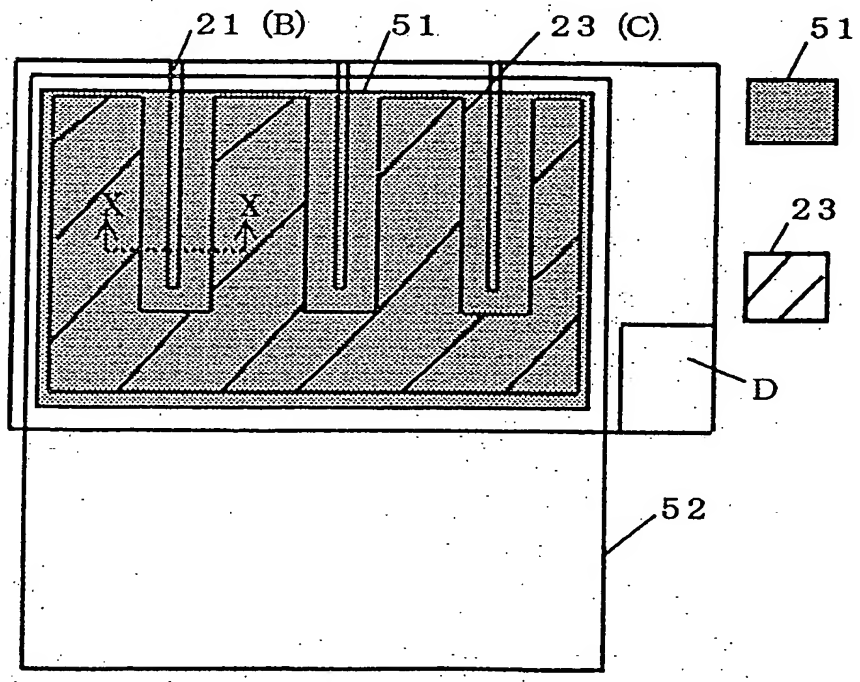
[Fig. 6]



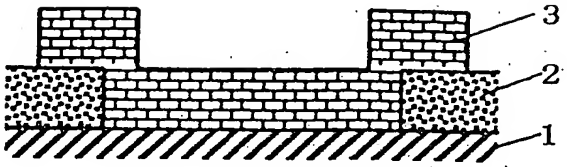
[Fig. 7]



[Fig. 8]



[Fig. 9]



[Fig. 10]